EC2354 VLSI DESIGN L T P C 3 0 0 3

UNIT I CMOS TECHNOLOGY 9
A brief History-MOS transistor, Ideal I-V characteristics, C-V characteristics, Non ideal IV effects, DC transfer characteristics - CMOS technologies, Layout design Rules, CMOS process enhancements, Technology related CAD issues, Manufacturing issues

UNIT II CIRCUIT CHARACTERIZATION AND SIMULATION 9
Delay estimation, Logical effort and Transistor sizing, Power dissipation, Interconnect, Design margin, Reliability, Scaling- SPICE tutorial, Device models, Device characterization, Circuit characterization, Interconnect simulation

UNIT III COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN 9
Circuit families –Low power logic design – comparison of circuit families – Sequencing static circuits, circuit design of latches and flip flops, Static sequencing element methodology- sequencing dynamic circuits – synchronizers

UNIT IV CMOS TESTING 9
Need for testing- Testers, Text fixtures and test programs- Logic verification- Silicon debug principles- Manufacturing test – Design for testability – Boundary scan

UNIT V SPECIFICATION USING VERILOG HDL 9
Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate level switch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Structural gate level description of decoder, equality detector, comparator, priority encoder, half adder, full adder, Ripple carry adder, D latch and D flip flop.

TOTAL= 45 PERIODS

TEXTBOOKS:

REFERENCES:
2 Wayne Wolf, Modern VLSI design, Pearson Education, 2003
3 M.J.S.Smith: Application specific integrated circuits, Pearson Education, 1997
4 J.Bhasker: Verilog HDL primer, BS publication,2001
5 Ciletti Advanced Digital Design with the Verilog HDL, Prentice Hall of India, 2003